Spartan 6 motherboard

Hardware manual

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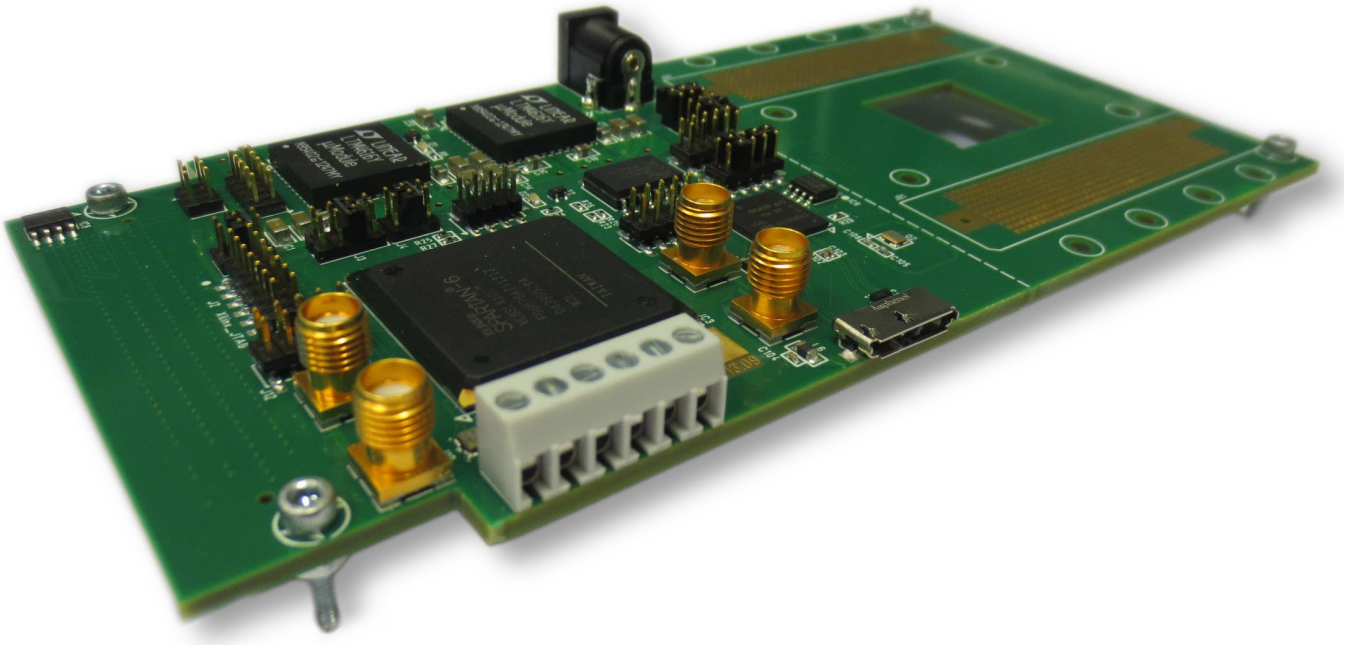

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Contents

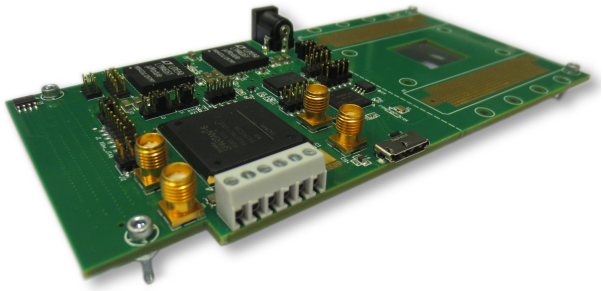
Chapter 1

Hardware

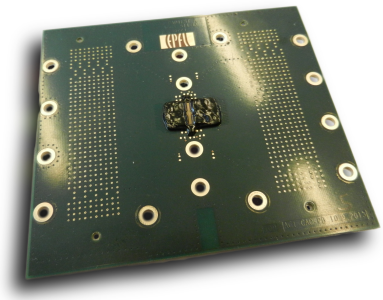
The system hardware consists of the following components (for the LinoSPAD system) and requirements for operation:

- LinoSPAD motherboard
- LinoSPAD daughterboard with the LinoSPAD chip
- Two power supplies for the LinoSPAD chip and wires to connect
- 5 V DC power jack
- USB3 cable with Micro-B plug
- (Digilent) FPGA Programming Cable

The components are shown in Figure 1.1.



(a) LinoSPAD mainboard.



(b) LinoSPAD daughterboard.

(c) Power supply.

(d) 5 V DC power jack.

(e) Micro-B USB3 cable.

(f) FPGA programming cable.

Figure 1.1: Overview of the hardware components.

The LinoSPAD motherboard is the base component, it is powered through the 5 V DC jack and connected to a host (PC) with the USB3 cable and the FPGA programming cable. A USB3 port is currently required as no backwards compatibility to USB2 has been implemented. The programming cable can be connected to a lower speed USB port.

On top of the motherboard, the daughterboard can be installed. For the chip, additional voltages are required. Therefore two additional power supplies are required to run the system with the LinoSPAD chip.

The motherboard is shown from the top in Figure 1.2, highlighting the different components on the board. The main components are the Xilinx Spartan 6 LX FPGA and the Cypress FX3 USB3 controller. The board fits Spartan 6 LX FPGAs in the FGG676 package. Current configurations use the LX100 and LX150. Furthermore power regulators and memories can be seen. The memories are used to store the firmware for the FPGA and FX3, so they do not have to be reloaded from the host after each power up.

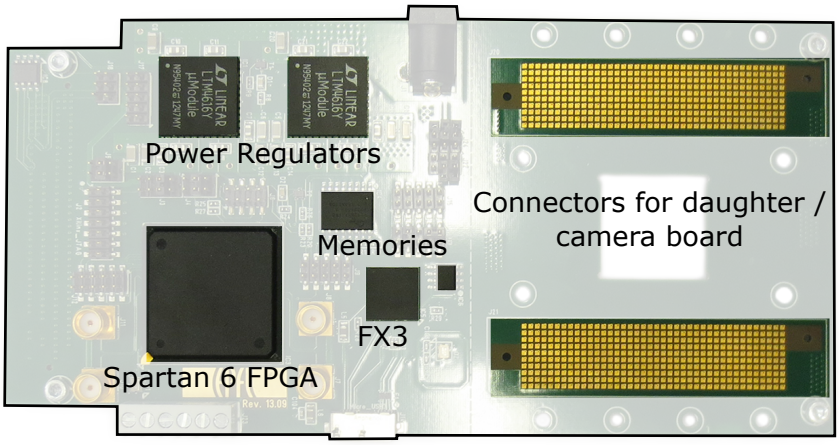


Figure 1.2: Different components on the LinoSPAD mainboard.

The (LX100) FPGA has 15,822 slices in which the logic can be placed, half of the slices contain carrychain structures (for TDCs). 286 16 kB RAM memories are available. There are maximum 480 pins to the outside world, they are connected with the FX3, the connectors for the daughterboard, a FMC interface to a secondary FPGA board and additional pins (as GPIO, SMA etc.).

For the I/O connectors, different voltages can be selected with a jumper: 3.3 V, 2.5 V and 1.8 V are available on board. Other jumpers are implemented to select between different boot modes for the FPGA and FX3. They can be set to load the firmware from the memory or to expect it from the host.

The FX3 is connected through a 32 bit bus with the FPGA, the maximum clock speed is 100 MHz. The maximum achieved speed was found to be around 300 MB/s depending on the host computer and programming.

1.1 Power

The board is powered from a 5V DC supply connected to J1. The four main power rails at 3.3V, 2.5V, 1.8V and 1.2V are generated by two LTM4616 switching regulator modules. The output capacity for each rail is 8A at an average efficiency of 85%. Diode D1 between the two regulator modules turns on when all rails are within +/-10% of their nominal value.

Additional power can be supplied to the daughterboard connected to J20 and J21. 3 of the four GFZ rails are connected to the screw terminal J23. All four GFZ rails for J20 and J21 are decoupled close to the connector with 1x $10\mu F$ and 2x $470nF$ 50V capacitors.

1.2 Configuration memories

Both, the Spartan 6 FPGA and the FX3, have SPI flash memories connected to hold configuration data.

A 16 MBit M25P16 flash memory with SPI interface is connected to the FX3. The FX3 is configured to boot from SPI flash memory by shorting pin pairs 1-3 and 7-8 on J13. The SPI memory is programmed through the FX3 using a firmware programmer previously downloaded to RAM when the FX3 is in bootloader mode after a failed SPI boot or direct USB boot. To get to the bootloader once the SPI flash is programmed USB boot can be selected by shorting pin pairs 1-3 and 5-6 on J13.

A 128 MBit S25FL128S flash memory with quad SPI interface is connected to the Spartan 6. The default mode pin configuration selects SPI master mode therefore only the chip-select has to be connected by placing a jumper on pins 1-2 of J9. Recent versions of the Xilinx iMPACT software support this memory and it can thus be programmed using a JTAG programmer. Diode D2 turns on when the FPGA is configured.

A 64 kBit 24LC64 flash memory with I2C interface is connected to the FMC connector. It can be used to store identifying information to use the card as FMC module. It can be programmed by the FMC carrier or through J17 with power on pin 3 of J18.

1.3 Oscillators

The FX3 uses a 19.2 MHz crystal from which it derives all its clocks. The FX3 can generate an interface clock which is fed to a clock input on the FPGA.

The Spartan 6 is connected to a 48 MHz crystal oscillator on a clock input of bank 0. It runs from 1.8 V to 3.3 V and can be used to generate other frequencies through the PLLs in the FPGA. J7, J8, J10 and J11 connect to clock capable inputs on the FPGA and can be used for single-ended or differential clocks to the FPGA.

1.4 Connectors and jumpers

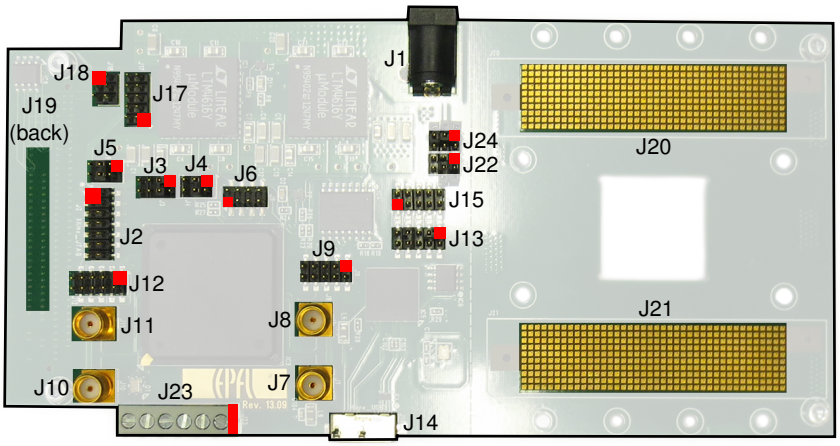


Figure 1.3: Connectors on the LinoSPAD mainboard. Non-keyed connectors have pin 1 marked red.

ID	Name	Description
J1	DC power	Center positive 5V DC supply. (power depending on application; suggested 20W)
J2	Xilinx JTAG	Standard pinout.

GND	1	2	2V5
GND	3	4	S6_TMS
GND	5	6	S6_TCK
GND	7	8	S6_TDO
GND	9	10	S6_TDI
GND	11	12	NC
GND	13	14	NC

ID	Name	Description
J3	FPGA Bank 0	Supplies J10, J11, J12 and J19
J4	FPGA Bank 1 & 5	I/O voltage for J20
J5	FPGA Bank 3 & 4	I/O voltage for J21
J6	FPGA startup	Power control and configuration override
J7	SMA 2V5 P	Positive clock input on FPGA 2.5V I/O
J8	SMA 2V5 N	Negative clock input on FPGA 2.5V I/O
J9	FPGA program	Miscellaneous programming pins
J10	SMA FMC P	Positive clock input on FPGA Bank 0 I/O
J11	SMA FMC N	Negative clock input on FPGA Bank 0 I/O
J12	FPGA GPIO	General purpose FPGA I/O on Bank 0
J13	FX3 startup	FX3 configuration mode selector
J14	Micro USB3	Micro USB3 Device connector
J15	FX3 debug	Miscellaneous pins for debugging
J17	FMC debug	Connection to FMC EEPROM and JTAG
J18	FMC power	Access to FMC power rails
J19	FMC module	FMC module connector; low pin count version; CLK0, CLK1 and differential pairs are connected; LX45 only 12 pairs, LX75 only 17 pairs
J20	Left GFZ	10 x 40 GFZ connector; 4 supply rails and up to 160 single-ended signals
J21	Right GFZ	10 x 40 GFZ connector; 4 supply rails and up to 160 single-ended signals
J22	GFZ_V0	Rail 0 for GFZ
J23	GFZ power	Connection to GFZ rails 1-3
J24	GFZ_V1	Rail 1 for GFZ

3V3	1	2	VCCO
2V5	3	4	VCCO
1V8	5	6	VCCO
FMC_VADJ	7	8	VCCO

3V3	1	2	VCCO
2V5	3	4	VCCO
1V8	5	6	VCCO

3V3	1	2	VCCO
2V5	3	4	VCCO
1V8	5	6	VCCO

PWR_RUN	1	2	GND
HSWAPEN	3	4	GND
M0	5	6	GND
M1	7	8	2V5

CSO_B	1	2	CSN
MISO_0	3	4	MISO_2
MISO_1	5	6	MISO_3
CCLK	7	8	PROGRAM_B
GND	9	10	2V5

PMODE_0	1	2	GND
2V5	3	4	GND
2V5	5	6	PMODE_1
PMODE_2	7	8	GND
2V5	9	10	CLKIN

FX3_TDI	1	2	I2C_SDA
FX3_TDO	3	4	I2C_SCL
FX3_TRSTN	5	6	GPIO_50
FX3_TMC	7	8	GPIO_51
FX3_TCK	9	10	GPIO_52

SCL	1	2	FMC_TCK
SDA	3	4	FMC_TDI
GA0	5	6	FMC_TDO
GA1	7	8	FMC_TMS
GND	9	10	FMC_TRSTN

FMC_3V3	1	2	FMC_3V3
FMC_3V3AUX	3	4	FMC_VADJ
GND	5	6	FMC_12V0

3V3	1	2	GFZ_V0
2V5	3	4	GFZ_V0
1V8	5	6	GFZ_V0

		1	GFZ_V1
		2	GND
		3	GFZ_V2
		4	GND
		5	GFZ_V3
		6	GND

1V2	1	2	GFZ_V1
5V0	3	4	GFZ_V1
FMC_12V0	5	6	GFZ_V1

1.4.1 GFZ daughtercard connectors

These connectors are to be used with Samtec® 10x40 GFZ spring connector arrays. The standard height of the connectors and therefore spacing between the PCBs is 3mm. The pinout is defined in figure Figure 1.4.

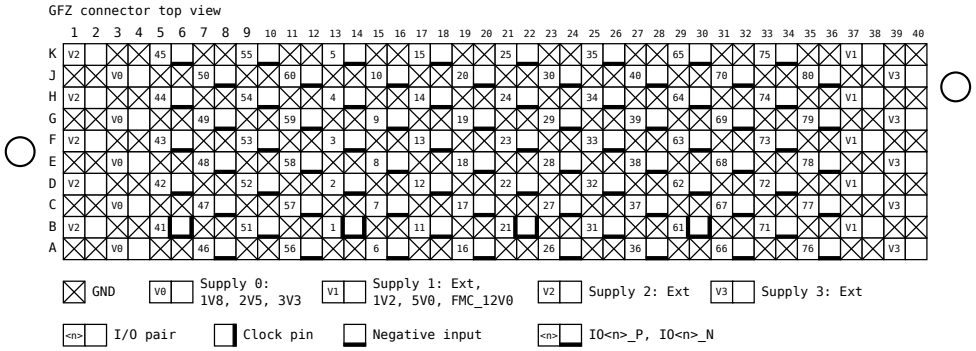


Figure 1.4: GFZ connector pinout.

1.5 Mechanical specifications

1.5.1 Motherboard

The motherboard is a standard FR4 PCB with 2mm thickness as outlined in figure Figure 1.5.

1.5.2 LinoSPAD daughterboard

The LinoSPAD PCB is 80mm x 70mm and fits to the top part of the motherboard. It is a PCB with 0.8mm to 1.2mm thickness and outline shown in figure Figure 1.7. Due to it being flexible it should be fixed with an additional plate on top or spacers between the PCBs to ensure good connections. The PCB is fixed to the motherboard using twelve M2.5 screws.

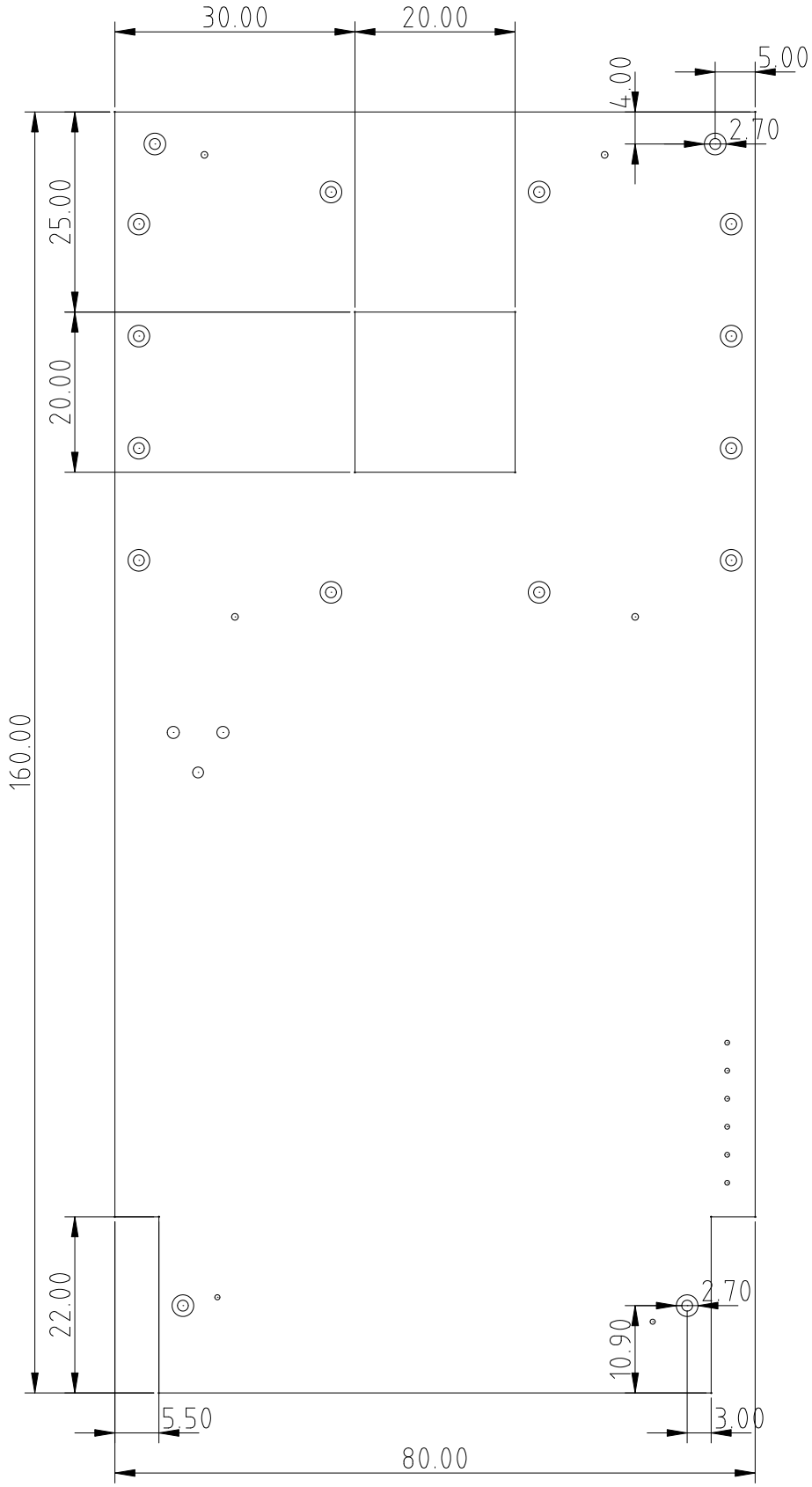


Figure 1.5: Motherboard mechanical drawing. The motherboard has four mounting holes in the corners. Additional dimensions for the daugherboard fixation are included in the daughterboard drawing.

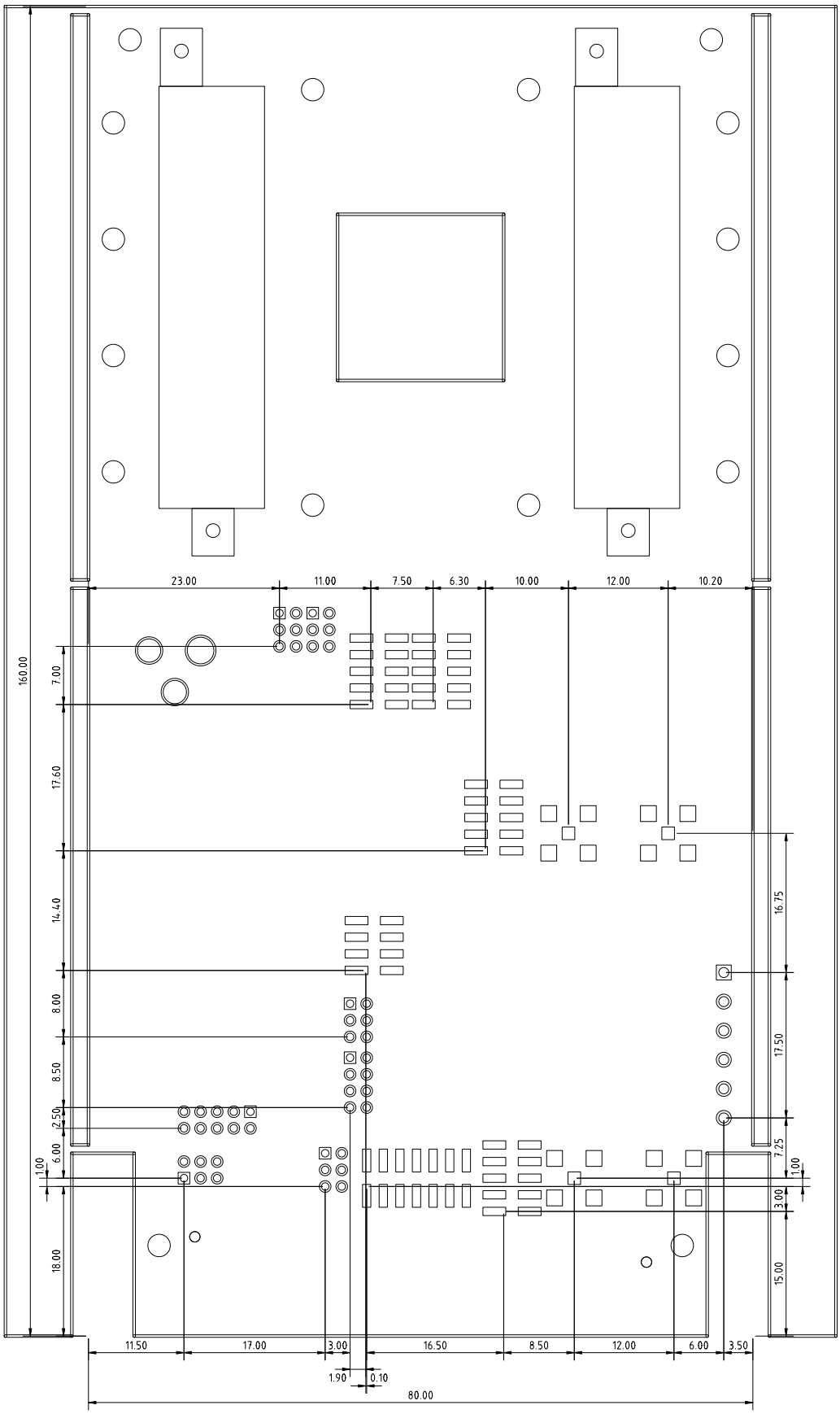


Figure 1.6: Motherboard pin header positions. Pin pitch is 2mm except for the screw terminal J23 where it is 3.5mm.

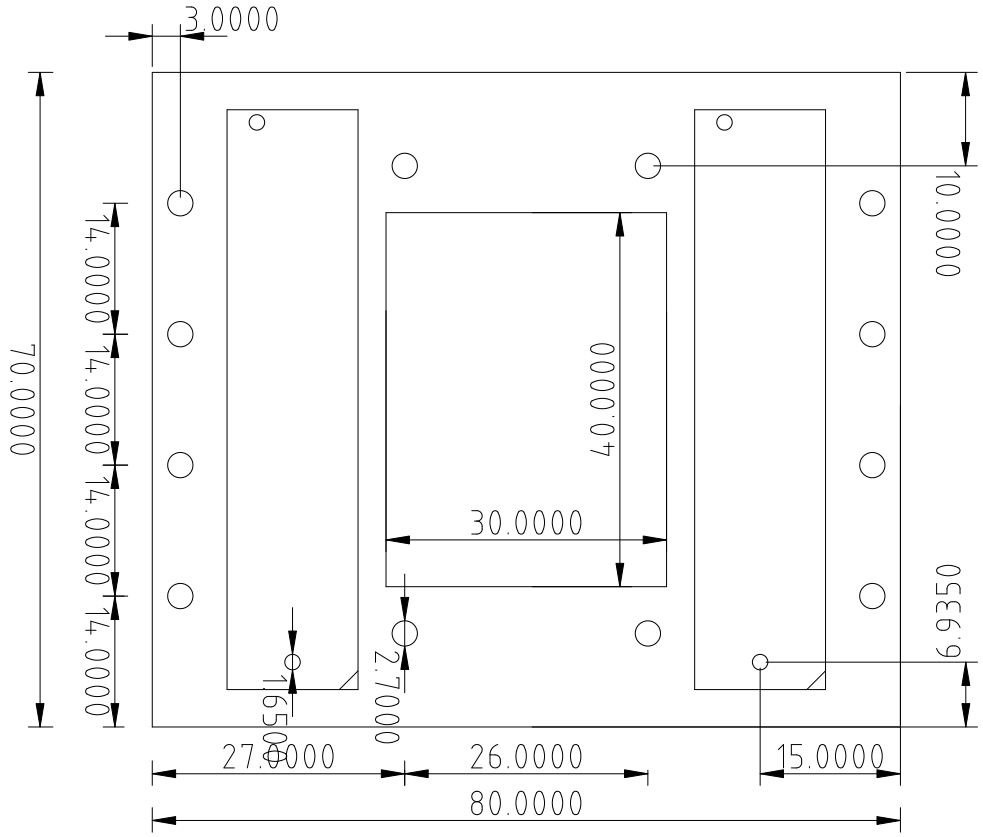


Figure 1.7: Daughterboard mechanical drawing.

1.6 Master user constraint file (.ucf)

This listing contains timing constraints and pin locations for all fixed Spartan 6 FPGA connections:

```
#Spartan 6 LX45-150 PCB rev. 13.09
###################################

#Bank 2 is fixed at 2.5V
CONFIG VCCAUX = 2.5;
#Banks 0,1,3,4,5 are selectable 1.8V - 3.3V

#Bank 0 is FMC, Osc and GPIO
#Bank 2 is FX3 and configuration
#Banks 1,5 are GFZ left
#Banks 3,4 are GFZ right

#Clock sources
#---------
#Bank 0
NET "OSC_48MHZ" LOC = C14;
NET "OSC_48MHZ" TNM_NET = "osc48";
TIMESPEC "TS_osc48" = PERIOD "osc48" 48 MHz HIGH 50 % INPUT_JITTER 80 ps;

NET "SMA_FMC_P" LOC = C15; #J10, bottom right
NET "SMA_FMC_N" LOC = A15; #J11, bottom left

#Bank 2
NET "SMA_2V5_P" LOC = AE13 | IOSTANDARD = LVCMOS25; #J7, top right
NET "SMA_2V5_N" LOC = AF13 | IOSTANDARD = LVCMOS25; #J8, top left

#FX3 (Bank 2)
#--------
NET "FX3*" IOSTANDARD = LVCMOS25 | DRIVE = 8 | FAST;

NET "FX3_PCLK" TNM_NET = "pclk100";
TIMESPEC "TS_pclk100" = PERIOD "pclk100" 100.8 MHz HIGH 50 %;

NET "FX3*" TNM = "FX3_TIMING";
TIMEGRP "FX3_TIMING" OFFSET = OUT 7 ns AFTER "FX3_PCLK" RISING VALID 3.5 ns;
TIMEGRP "FX3_TIMING" OFFSET = IN 2 ns BEFORE "FX3_PCLK" RISING VALID 4 ns;

NET "FX3_PCLK" LOC = AD12;
NET "FX3_RESET_N" LOC = AD8;

NET "FX3_SLCS_N" LOC = AA15;
NET "FX3_SLOE_N" LOC = AE21;
NET "FX3_SLRD_N" LOC = AD18;
NET "FX3_SLWR_N" LOC = AB15;
NET "FX3_PKTEND_N" LOC = AF19;

NET "FX3_FLAG_A" LOC = AD10;
NET "FX3_FLAG_B" LOC = AE15;
NET "FX3_FLAG_C" LOC = AC15;
NET "FX3_FLAG_D" LOC = AD15;

NET "FX3_FIFOADR[0]" LOC = AB17;
NET "FX3_FIFOADR[1]" LOC = AF16;

NET "FX3_GPIO[0]" LOC = AF15; #GPIO[26]
NET "FX3_GPIO[1]" LOC = AC17; #GPIO[27]
#NET "FX3_CTL[15]" LOC = AC14;

NET "FX3_DQ[0]" LOC = AE9;
NET "FX3_DQ[1]" LOC = AF18;
NET "FX3_DQ[2]" LOC = AF9;
NET "FX3_DQ[3]" LOC = AF11;
NET "FX3_DQ[4]" LOC = AE11;
NET "FX3_DQ[5]" LOC = AF8;
NET "FX3_DQ[6]" LOC = AA12;
NET "FX3_DQ[7]" LOC = AE19;
NET "FX3_DQ[8]" LOC = AC12;
NET "FX3_DQ[9]" LOC = W12;
NET "FX3_DQ[10]" LOC = AB13;
NET "FX3_DQ[11]" LOC = V12;
NET "FX3_DQ[12]" LOC = AA13;
NET "FX3_DQ[13]" LOC = Y15;
NET "FX3_DQ[14]" LOC = AF21;
NET "FX3_DQ[15]" LOC = AF10;
#Not connected on LX75
NET "FX3_DQ[16]" LOC = AB18;
NET "FX3_DQ[17]" LOC = AA18;
NET "FX3_DQ[18]" LOC = AD19;
NET "FX3_DQ[19]" LOC = AC19;
NET "FX3_DQ[20]" LOC = AD17;
NET "FX3_DQ[21]" LOC = AA19;
NET "FX3_DQ[22]" LOC = AC20;
NET "FX3_DQ[23]" LOC = AA17;
NET "FX3_DQ[24]" LOC = AC16;
NET "FX3_DQ[25]" LOC = AD21;
NET "FX3_DQ[26]" LOC = Y18;
NET "FX3_DQ[27]" LOC = V16;
NET "FX3_DQ[28]" LOC = Y16;
NET "FX3_DQ[29]" LOC = W17;
NET "FX3_DQ[30]" LOC = V15;
NET "FX3_DQ[31]" LOC = W16;

#SPI Flash
#------
```

```
NET "SPI*" IOSTANDARD = LVCMOS25 | DRIVE = 8 | FAST;
NET "SPI_CSN" LOC = AF4;
NET "SPI_SCK" LOC = AD22;
NET "SPI_MOSI" LOC = AF20;
NET "SPI_MISO" LOC = AD20;
NET "SPI_WPN" LOC = AE17 | PULLUP;
NET "SPI_HOLDN" LOC = AF17 | PULLUP;

#GPIO (Bank 0)
#---------
#13.09: GPIO[0;1] not connected on LX45,75
NET "GPIO[0]" LOC = H17;
NET "GPIO[1]" LOC = J17;
NET "GPIO[2]" LOC = A18;
NET "GPIO[3]" LOC = B18;
NET "GPIO[4]" LOC = A19;
NET "GPIO[5]" LOC = C19;
NET "GPIO[6]" LOC = A20;
NET "GPIO[7]" LOC = B20;
NET "GPIO[8]" LOC = A21;
NET "GPIO[9]" LOC = C21;

#GFZ left (Bank 1,5) #56-#73 not connected on LX45
#---------------------------------
NET "GFZ_LP[1]" LOC = P21;
NET "GFZ_LP[2]" LOC = D24;
NET "GFZ_LP[3]" LOC = B24;
NET "GFZ_LP[4]" LOC = C25;
NET "GFZ_LP[5]" LOC = B25;
NET "GFZ_LP[6]" LOC = N17;
NET "GFZ_LP[7]" LOC = M18;
NET "GFZ_LP[8]" LOC = R20;
NET "GFZ_LP[9]" LOC = T18;
NET "GFZ_LP[10]" LOC = B23;
NET "GFZ_LP[11]" LOC = T23;
NET "GFZ_LP[12]" LOC = R23;
NET "GFZ_LP[13]" LOC = U17;
NET "GFZ_LP[14]" LOC = V18;
NET "GFZ_LP[15]" LOC = M23;
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NET "GFZ_LP[61]" LOC = U25;
NET "GFZ_LP[62]" LOC = J23;
NET "GFZ_LP[63]" LOC = H20;
NET "GFZ_LP[64]" LOC = H22;
NET "GFZ_LP[65]" LOC = G20;
NET "GFZ_LP[66]" LOC = K20;
NET "GFZ_LP[67]" LOC = L20;
NET "GFZ_LP[68]" LOC = K22;
NET "GFZ_LP[69]" LOC = R22;
NET "GFZ_LP[70]" LOC = AB21;
NET "GFZ_LP[71]" LOC = H19;
NET "GFZ_LP[72]" LOC = P17;
NET "GFZ_LP[73]" LOC = R17;

NET "GFZ_LN[1]" LOC = P22;
```

```
NET "GFZ_LN[2]" LOC = D26;
NET "GFZ_LN[3]" LOC = A25;
NET "GFZ_LN[4]" LOC = C26;
NET "GFZ_LN[5]" LOC = B26;
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NET "GFZ_LN[61]" LOC = U26;
NET "GFZ_LN[62]" LOC = J24;
NET "GFZ_LN[63]" LOC = H21;
NET "GFZ_LN[64]" LOC = G22;
NET "GFZ_LN[65]" LOC = G21;
NET "GFZ_LN[66]" LOC = K21;
NET "GFZ_LN[67]" LOC = L21;
NET "GFZ_LN[68]" LOC = J22;
NET "GFZ_LN[69]" LOC = R21;
NET "GFZ_LN[70]" LOC = AB22;
NET "GFZ_LN[71]" LOC = J20;
NET "GFZ_LN[72]" LOC = P18;
NET "GFZ_LN[73]" LOC = R18;

#GFZ right (Bank 3,4) #56-#73 not connected on LX45
#---------------------------------
NET "GFZ_RP[1]" LOC = V4;
NET "GFZ_RP[2]" LOC = V3;
NET "GFZ_RP[3]" LOC = L2;
NET "GFZ_RP[4]" LOC = L4;
NET "GFZ_RP[5]" LOC = M3;
NET "GFZ_RP[6]" LOC = U2;
NET "GFZ_RP[7]" LOC = U4;
NET "GFZ_RP[8]" LOC = N2;
NET "GFZ_RP[9]" LOC = N7;
NET "GFZ_RP[10]" LOC = N4;
NET "GFZ_RP[11]" LOC = R4;
NET "GFZ_RP[12]" LOC = R5;
NET "GFZ_RP[13]" LOC = P7;
NET "GFZ_RP[14]" LOC = U8;
NET "GFZ_RP[15]" LOC = P3;
NET "GFZ_RP[16]" LOC = R7;
NET "GFZ_RP[17]" LOC = P10;
NET "GFZ_RP[18]" LOC = AE3;
NET "GFZ_RP[19]" LOC = AC5;
NET "GFZ_RP[20]" LOC = AC4;
NET "GFZ_RP[21]" LOC = T3;
NET "GFZ_RP[22]" LOC = M9;
NET "GFZ_RP[23]" LOC = M10;
NET "GFZ_RP[24]" LOC = AB7;
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NET "GFZ_RP[25]" LOC = AA7;
NET "GFZ_RP[26]" LOC = M6;
NET "GFZ_RP[27]" LOC = L7;
NET "GFZ_RP[28]" LOC = AA4;
NET "GFZ_RP[29]" LOC = AA2;
NET "GFZ_RP[30]" LOC = AB3;
NET "GFZ_RP[31]" LOC = P5;
NET "GFZ_RP[32]" LOC = AB4;
NET "GFZ_RP[33]" LOC = AC2;
NET "GFZ_RP[34]" LOC = AE2;
NET "GFZ_RP[35]" LOC = AD3;
NET "GFZ_RP[36]" LOC = W5;
NET "GFZ_RP[37]" LOC = W8;
NET "GFZ_RP[38]" LOC = AC7;
NET "GFZ_RP[39]" LOC = T8;
NET "GFZ_RP[40]" LOC = AA5;
NET "GFZ_RP[41]" LOC = N8;
NET "GFZ_RP[42]" LOC = H3;
NET "GFZ_RP[43]" LOC = J2;
NET "GFZ_RP[44]" LOC = K3;
NET "GFZ_RP[45]" LOC = U5;
NET "GFZ_RP[46]" LOC = E4;
NET "GFZ_RP[47]" LOC = F3;
NET "GFZ_RP[48]" LOC = E2;
NET "GFZ_RP[49]" LOC = G2;
NET "GFZ_RP[50]" LOC = W2;
NET "GFZ_RP[51]" LOC = C4;
NET "GFZ_RP[52]" LOC = D3;
NET "GFZ_RP[53]" LOC = C2;
NET "GFZ_RP[54]" LOC = B2;
NET "GFZ_RP[55]" LOC = Y3;
NET "GFZ_RP[56]" LOC = H8;
NET "GFZ_RP[57]" LOC = J7;
NET "GFZ_RP[58]" LOC = W9;
NET "GFZ_RP[59]" LOC = K10;
NET "GFZ_RP[60]" LOC = J10;
NET "GFZ_RP[61]" LOC = R2;
NET "GFZ_RP[62]" LOC = K7;
NET "GFZ_RP[63]" LOC = R10;
NET "GFZ_RP[64]" LOC = V7;
NET "GFZ_RP[65]" LOC = T10;
NET "GFZ_RP[66]" LOC = K5;
NET "GFZ_RP[67]" LOC = J4;
NET "GFZ_RP[68]" LOC = K8;
NET "GFZ_RP[69]" LOC = Y9;
NET "GFZ_RP[70]" LOC = W10;
NET "GFZ_RP[71]" LOC = G6;
NET "GFZ_RP[72]" LOC = G4;
NET "GFZ_RP[73]" LOC = F5;
NET "GFZ_RP[74]" LOC = H6;
NET "GFZ_RP[75]" LOC = AA8;

NET "GFZ_RN[1]" LOC = W3;
NET "GFZ_RN[2]" LOC = V1;
NET "GFZ_RN[3]" LOC = L1;
NET "GFZ_RN[4]" LOC = L3;
NET "GFZ_RN[5]" LOC = M1;
NET "GFZ_RN[6]" LOC = U1;
NET "GFZ_RN[7]" LOC = U3;
NET "GFZ_RN[8]" LOC = N1;
NET "GFZ_RN[9]" LOC = N6;
NET "GFZ_RN[10]" LOC = N3;
NET "GFZ_RN[11]" LOC = R3;
NET "GFZ_RN[12]" LOC = T4;
NET "GFZ_RN[13]" LOC = P6;
NET "GFZ_RN[14]" LOC = U7;
NET "GFZ_RN[15]" LOC = P1;
NET "GFZ_RN[16]" LOC = R6;
NET "GFZ_RN[17]" LOC = R9;
NET "GFZ_RN[18]" LOC = AF2;
NET "GFZ_RN[19]" LOC = AD5;
NET "GFZ_RN[20]" LOC = AD4;
NET "GFZ_RN[21]" LOC = T1;
NET "GFZ_RN[22]" LOC = M8;
NET "GFZ_RN[23]" LOC = N9;
NET "GFZ_RN[24]" LOC = AB6;
NET "GFZ_RN[25]" LOC = Y6;
NET "GFZ_RN[26]" LOC = M4;
NET "GFZ_RN[27]" LOC = L6;
NET "GFZ_RN[28]" LOC = AA3;
NET "GFZ_RN[29]" LOC = AA1;
NET "GFZ_RN[30]" LOC = AB1;
NET "GFZ_RN[31]" LOC = N5;
NET "GFZ_RN[32]" LOC = AC3;
NET "GFZ_RN[33]" LOC = AC1;
NET "GFZ_RN[34]" LOC = AE1;
NET "GFZ_RN[35]" LOC = AD1;
NET "GFZ_RN[36]" LOC = Y5;
NET "GFZ_RN[37]" LOC = W7;
NET "GFZ_RN[38]" LOC = AD7;
NET "GFZ_RN[39]" LOC = T6;
NET "GFZ_RN[40]" LOC = AB5;
NET "GFZ_RN[41]" LOC = P8;
NET "GFZ_RN[42]" LOC = H1;
NET "GFZ_RN[43]" LOC = J1;
NET "GFZ_RN[44]" LOC = K1;
NET "GFZ_RN[45]" LOC = V5;
NET "GFZ_RN[46]" LOC = E3;
NET "GFZ_RN[47]" LOC = F1;
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NET "GFZ_RN[48]" LOC = E1;
NET "GFZ_RN[49]" LOC = G1;
NET "GFZ_RN[50]" LOC = W1;
NET "GFZ_RN[51]" LOC = C3;
NET "GFZ_RN[52]" LOC = D1;
NET "GFZ_RN[53]" LOC = C1;
NET "GFZ_RN[54]" LOC = B1;
NET "GFZ_RN[55]" LOC = Y1;
NET "GFZ_RN[56]" LOC = G7;
NET "GFZ_RN[57]" LOC = H7;
NET "GFZ_RN[58]" LOC = V8;
NET "GFZ_RN[59]" LOC = L9;
NET "GFZ_RN[60]" LOC = K9;
NET "GFZ_RN[61]" LOC = R1;
NET "GFZ_RN[62]" LOC = K6;
NET "GFZ_RN[63]" LOC = T9;
NET "GFZ_RN[64]" LOC = V6;
NET "GFZ_RN[65]" LOC = U9;
NET "GFZ_RN[66]" LOC = J5;
NET "GFZ_RN[67]" LOC = J3;
NET "GFZ_RN[68]" LOC = L8;
NET "GFZ_RN[69]" LOC = Y8;
NET "GFZ_RN[70]" LOC = V10;
NET "GFZ_RN[71]" LOC = G5;
NET "GFZ_RN[72]" LOC = G3;
NET "GFZ_RN[73]" LOC = E5;
NET "GFZ_RN[74]" LOC = H5;
NET "GFZ_RN[75]" LOC = AB8;

#FMC LPC (Bank 0)
#-----------
NET "FMC_CLK_M2C_P[0]" LOC = B14;
NET "FMC_CLK_M2C_N[0]" LOC = A14;
NET "FMC_CLK_M2C_P[1]" LOC = C13;
NET "FMC_CLK_M2C_N[1]" LOC = A13;

NET "FMC_LA_P[0]" LOC = B12;
NET "FMC_LA_N[0]" LOC = A12;
NET "FMC_LA_P[1]" LOC = B8;
NET "FMC_LA_N[1]" LOC = A8;
NET "FMC_LA_P[2]" LOC = C11;
NET "FMC_LA_N[2]" LOC = A11;
NET "FMC_LA_P[3]" LOC = C9;
NET "FMC_LA_N[3]" LOC = A9;
NET "FMC_LA_P[4]" LOC = C7;
NET "FMC_LA_N[4]" LOC = A7;
NET "FMC_LA_P[5]" LOC = C5;
NET "FMC_LA_N[5]" LOC = A5;
NET "FMC_LA_P[6]" LOC = D6;
NET "FMC_LA_N[6]" LOC = C6;
NET "FMC_LA_P[7]" LOC = B4;
NET "FMC_LA_N[7]" LOC = A4;
NET "FMC_LA_P[8]" LOC = B6;
NET "FMC_LA_N[8]" LOC = A6;
NET "FMC_LA_P[9]" LOC = D21;
NET "FMC_LA_N[9]" LOC = C20;
NET "FMC_LA_P[10]" LOC = B16;
NET "FMC_LA_N[10]" LOC = A16;
NET "FMC_LA_P[11]" LOC = D18;
NET "FMC_LA_N[11]" LOC = C18;
NET "FMC_LA_P[12]" LOC = C17;
NET "FMC_LA_N[12]" LOC = A17;
#Not connected on LX45
NET "FMC_LA_P[13]" LOC = B10;
NET "FMC_LA_N[13]" LOC = A10;
NET "FMC_LA_P[14]" LOC = G8;
NET "FMC_LA_N[14]" LOC = F7;
NET "FMC_LA_P[15]" LOC = F17;
NET "FMC_LA_N[15]" LOC = E17;
NET "FMC_LA_P[16]" LOC = J15;
NET "FMC_LA_N[16]" LOC = H15;
NET "FMC_LA_P[17]" LOC = F16;
NET "FMC_LA_N[17]" LOC = E16;
#Not connected on LX45,75
NET "FMC_LA_P[18]" LOC = F9;
NET "FMC_LA_N[18]" LOC = E9;
NET "FMC_LA_P[19]" LOC = D10;
NET "FMC_LA_N[19]" LOC = C10;
NET "FMC_LA_P[20]" LOC = E10;
NET "FMC_LA_N[20]" LOC = F10;
NET "FMC_LA_P[21]" LOC = D12;
NET "FMC_LA_N[21]" LOC = C12;
NET "FMC_LA_P[22]" LOC = D11;
NET "FMC_LA_N[22]" LOC = F11;
NET "FMC_LA_P[23]" LOC = D8;
NET "FMC_LA_N[23]" LOC = C8;
NET "FMC_LA_P[24]" LOC = J14;
NET "FMC_LA_N[24]" LOC = G14;
NET "FMC_LA_P[25]" LOC = F13;
NET "FMC_LA_N[25]" LOC = D13;
NET "FMC_LA_P[26]" LOC = E6;
NET "FMC_LA_N[26]" LOC = D5;
NET "FMC_LA_P[27]" LOC = E8;
NET "FMC_LA_N[27]" LOC = D7;
NET "FMC_LA_P[28]" LOC = G16;
NET "FMC_LA_N[28]" LOC = F15;
NET "FMC_LA_P[29]" LOC = E14;
NET "FMC_LA_N[29]" LOC = D15;
NET "FMC_LA_P[30]" LOC = H16;
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NET "FMC_LA_N[30]" LOC = G17;
NET "FMC_LA_P[31]" LOC = D16;
NET "FMC_LA_N[31]" LOC = C16;
NET "FMC_LA_P[32]" LOC = E19;
NET "FMC_LA_N[32]" LOC = D19;
NET "FMC_LA_P[33]" LOC = F18;
NET "FMC_LA_N[33]" LOC = E18;
```

1.7 Hardware revisions

1.7.1 Revision 13.09

Minor issues have been identified with this revision of the LinoSPAD motherboard.

- For the two LEDs to work the transistors T1 and T2 need to be soldered on their back, such that two pins are exchanged.
- For the FX3 to configure correctly from the flash memory the resistor R40 on the back needs to be removed.
- For the Spartan 6 to use the flash memory a jumper wire has to be soldered from J9 pin 2 to the chip select of the memory, pin 7 of IC4 or the left side of R20.